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AMENDMENT TO THE SPECIFICATION

Please amend the specification as follows:

[00022] FIG. 1 is a block diagram illustrating a computer system 100 including a dynamic binary translator 300, in accordance with one embodiment of the invention. As illustrated, computer system 100 includes a processor (CPU) 110, memory 140 and an optional graphics controller 130 coupled to memory controller hub (MCH) 120. Representatively, CPU 110 is coupled to chipset 180 via front side bus (FSB) 102. Likewise, chipset 180 is coupled to memory 140 via interconnect 142 and graphics controller 130 is coupled to chipset 180 via interconnect 132. As described herein, MCH 120 may be referred to as a north bridge and, in one embodiment, as a memory controller. In an alternate embodiment, MCH 120 may be implemented within CPU 110. In addition, computer system 100 includes I/O (input/output) controller hub (ICH) 160 is coupled to MCH 120 via interconnect 106. As described herein ICH 160 may be referred to as a south bridge or I/O controller. South bridge, or ICH 160, is coupled to I/O devices 150 (150-1, . . ., 150-N) and hard disk drive devices (HDD) ~~160~~ 104.

[00044] FIG. 9 is a flowchart illustrating a method 440 for, for example, processing one of a segment table update instruction and a segment register update instruction within a source ISA application. At process block ~~432~~442, each segment descriptor within the target segment table is identified. Once identified, at process block 444, a target register is assigned to each segment described by an identified segment descriptor. At process block 446, a base address of each segment descriptor is loaded within the target register assigned to the segment corresponding to the segment descriptor.